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... of the basic LUT as a Shift Register (SRL16) or as a SelectRAM+™ memory and the ... comparator size. Figure 1 compares a RAM and a CAM in read mode. ...

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... bus before the end of the current cycle (one clock cycle earlier). ... more programs to be stored in memory for a given RAM size than segmentation. ...

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... largest block size and the number of words in the LUT is ... interleaver the

data memory size is 288 (maximum block ...

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... look-up table section and SRAM as the packet buffer memory. ...

The memory

size increases dramatically to 2400 Mbits of TCAM for IPv6 with the same ...

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... The coefficient memory consists of a ROM, a look-up table (LUT), an address counter, ... and write accesses to the memory every clock cycle. Therefore, ...

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... changing some parameters in the programs (FPGA size, **memory size** in FPGA, ...
for one **clock cycle** to compare elements on the next diagonal lines as ...

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... All **memory** access operations complete in one **clock cycle** ... bits computed in
one **clock cycle**. Clock period increases logarithmically with row **size** ...

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... that takes only two clock cycles to sort data, regardless of **size**. ...

each line of source code into hardware that executes in a single **clock cycle**. ...

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... A single read or write cycle involves a single 2n-bit wide, one-clock-cycle data

... that only uses internal routing and **look-up-table** delay with a ...

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... which is sampled during the last **clock cycle** of each instruction to determine if ... A subroutine is vectored to via an interrupt vector **look-up table** ...

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... these are the four most significant address lines for **memory operations**. ... enable FLAG bit (S5) is updated at the beginning of each **clock cycle**. ...

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... After the first **clock cycle**, the tail pointer is masked out and sent to the ... Alternatively, an external **look-up table** (LUT) can be used to initialize ...

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... mode, each element acts as a **lookup table** that allows. the cell to implement a wide variety ... multiplication per **clock cycle**. The clock frequency is ...

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... can act as a **lookup table** or a small memory. As discussed ... **memory operations**, the other optimized for mathematical ... operation every **clock cycle**. ...

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... "In addition to instructions that support pure memory to **memory operations**, ... this is done using an algorithm based on a **lookup table** that resides in ...

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... Figure 7: IP **lookup table** represented as a binary trie. ... data path width and 4 **clock cycle** latency of the memory. suggest an optimal stride length of ...

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... major **clock cycle**. The high-speed execution core, controlled ... The CLB is a CAM used as a **lookup table** for the TCP con-. nections. ...

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... beginning of each **clock cycle** S4 and S3 are encoded as shown ... subroutine is vectored to via an interrupt vector **lookup table** located in ...

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... Since across-chip interconnect delays can exceed a **clock cycle** in ... up table (LUT), indexed by the set of bus latencies, is constructed ...

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